What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate having a channel region and an impurity region disposed at both sides of the channel region;

a first polysilicon layer disposed on a surface of the channel region;

a gate oxide film disposed between the first polysilicon layer and the surface of the channel region and extending laterally to have a width larger than that of the first polysilicon film, wherein a thickness of the edge of the gate oxide film is larger than that of the center portion thereof so as to surround side walls of the first polysilicon film;

a gate electrode, disposed on the first polysilicon film, comprising a metal layer and a second polysilicon layer surrounding the metal layer; and

an insulating film spacer disposed on both sides of the gate electrode.

2. A semiconductor device according to the claim 1, wherein the gate oxide film is a thermal oxide film.

3. A semiconductor device according to the claim 1, wherein the gate oxide film consists of SiO_2, SiN or Ta_2O_5.

4. A semiconductor device according to the claim 1, wherein the impurity region comprises a low concentration impurity region extending from the both ends of the channel region and a high concentration impurity region extending from both sides of the a low concentration impurity region.

5. A semiconductor device according to the claim 4, wherein the low and the high concentration impurity regions are ion-implanted with a ion having a first conductive type, and the channel region is ion-implanted with a ion having a second conductive type, the first conductive type being an opposite conductive type to the second conductive type.

6. A semiconductor device according to the claim 1, wherein the metal layer consists of W or Al.

7. A method for manufacturing a semiconductor device comprising the steps of:

providing a semiconductor substrate having an element isolating film defining an active region;

forming a dummy gate comprising a gate oxide film, a

first polysilicon layer and a hard mask layer sequentially stacked on the active region;

performing a thermal oxidation process to the overall surface to form a thermal oxide film on the sidewalls of the first polysilicon layer and on the both sides of the gate oxide film, wherein the thermal oxidation film on the both sides of the gate oxide film is thicker than the gate oxide film;

forming a low concentration impurity region by performing a first ion implantation process on the entire surface including the dummy gate;

forming an insulating film over the resulting structure;

etching back the insulating film and the thermal oxide film on the semiconductor substrate to form an insulating film spacer on the sidewall of the dummy gate;

forming a high concentration impurity region in the semiconductor substrate on the both sides of the dummy gate electrode by performing a second ion implantation process;

forming a planarized interlayer insulating film for exposing the upper portion of the dummy gate;

removing the hard mask layer to form groove exposing the first polysilicon layer;

forming a Vth ion implantation region in a channel region of the semiconductor substrate by performing a third

ion implantation process;

subjecting the resultant structure to a thermal annealing process;

sequentially forming a second polysilicon layer on the entire surface and a metal layer filling the groove;

etching back the metal layer to form a recessed metal pattern in the groove;

forming a third polysilicon layer overall surface of the resulting structure so as to fill the recess region in the groove; and

planarizing the resultant to expose the interlayer insulating film.

8. The method according to claim 7, wherein the gate oxide film is a silicon oxide film, a silicon nitride film or a tantalum oxide film.

9. The method according to claim 7, wherein dopant used in the first and the second ion implantation processes is N-type or P-type.

10. The method according to claim 7, wherein the polarities of the dopants used in the first and third ion implantation process are opposite each other.

ion implantation region is formed on the surface of the center portion of the channel region.

12. The method according to claim 7, wherein the hard mask layer comprises a nitride film.

13. The method according to claim 7, wherein the step of removing the hard mask is performed by dry etching process.

14. The method according to claim 7, wherein the metal layer is tungsten or aluminum layer.